AMENDMENTS TO THE DRAWINGS

One Replacement Sheet of drawings, to be substituted for the corresponding drawing sheet presently on file, is submitted herewith.

REMARKS

This application has been reviewed in light of the Office Action dated July 28, 2005.

Claims 1-21 are now presented for examination. Claims 1, 3-5, 12, 13, 18, 20 and 21 have been amended to more particularly point out and distinctly claim the subject matter regarded as the invention. Claims 1, 12, 18 and 20 are independent. Favorable review is respectfully requested.

The Examiner objected to the drawings, stating that "Figure 2 has an edge (D-F) containing both solid and dotted lines." The Examiner is evidently referring to Figure 2A, which depicts a circuit having critical and non-critical timing paths, shown as solid and dotted lines respectively (see specification, para. 0043). Figure 2A has been carefully reviewed and redrawn so that solid and dotted lines are distinct from each other. A Replacement Sheet of drawings, which includes the revised Figure 2A, is submitted herewith.

Claims 1, 5 and 18 were objected to, the Examiner stating that the term "critical" should be added in those claims before "path associated." Claims 1, 5 and 18 have been amended to change "path associated" to –critical path associated— wherever that phrase appears.

Claim 16 was also objected to, the Examiner stating that it was not certain whether claim 16 was meant to depend from claim 1 or from claim 12. The applicants confirm that claim 16 depends from claim 1. It is noted that claim 17 recites the same language as claim 16 and depends from claim 12.

Claims 1-21 were rejected under 35 U.S.C. § 102(b) as being anticipated by Greidinger et al. (U.S. Pat. No. 6,449,761). The applicants respectfully submit that amended independent claims 1, 12, 18 and 20 are patentably distinct from the cited art, for the following reasons.

The present invention, as defined in claim 1, is directed to a method for optimizing design of a microelectronic circuit using a plurality of processors. It is a feature of the invention that the optimizing is performed in parallel by the processors. (This feature is also explicitly recited in claim 18 and in amended claims 12 and 20.) In the method of claim 1, a

set of endpoints of critical paths is partitioned in accordance with predetermined rules regarding timing independence and geometric independence. As taught in the specification (see e.g. para. 0045 and 0047), partitioning the set of endpoints in this fashion permits efficient optimization by parallel processors.

Claim 12 also recites a partitioning step, in which an endpoint graph is partitioned in accordance with timing independence and geometric independence rules. Claims 18 and 20 are directed to a computer-readable storage medium having instructions stored therein for performing methods as recited in claims 1 and 12 respectively.

It is thus a feature of the present invention that (1) optimization of the circuit is performed by parallel processors; and (2) each processor optimizes a different sub-set of paths (claims 1, 18) or paths associated with a different sub-set of vertices of a graph (claims 12, 20).

Greidinger et al. is understood to disclose an EDA system in which the user may specify various constraints (topological, net, and timing), and a circuit is optimized in accordance with those constraints. The applicants cannot find in Greidinger et al.'s discussion of constraints (col. 7, lines 34-63) any disclosure or suggestion of a timing independence rule or geometric independence rule as in the present invention. Furthermore, there is no suggestion, let alone an explicit teaching, of any relationship between such rules and the use of parallel processors, as in the present invention. Accordingly, Greidinger et al. does not teach a step of partitioning as in the present invention.

The applicants wish to point out that "partitioning," as used throughout the specification and claims, refers to a process of defining sub-sets of objects (critical paths, or vertices of a graph) to permit optimization using parallel processors. This is a logical process, not a physical process, and should not be confused with the "cuts" or physical node removals of Greidinger et al.

The Examiner points to claim 14 of Greidinger et al. for a disclosure of optimization by parallel processors. The applicants wish to point out that the claim merely recites "one or more" processors, and does not suggest any processing in parallel. There is also no mention in the claim of any method by which the set of critical paths in the circuit layout might be

partitioned. Indeed, Greidinger et al. suggests (col. 14, lines 1-16) that all the cuts in the layout are made in a linear fashion, in order according to cost. The applicants have not found any disclosure or suggestion that this process may be performed by parallel processors, or what rules should be invoked to permit parallel processing.

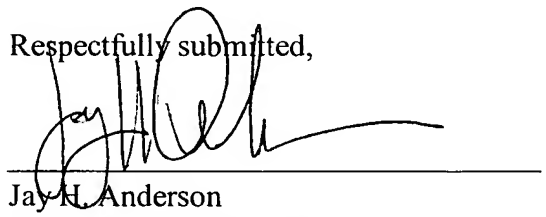
Accordingly, it is submitted that Greidinger et al. does not disclose the above-described features of the present invention, so that the present invention is not anticipated by that reference.

The other claims in this application are each dependent directly or indirectly from one or another of the independent claims discussed above and are therefore also believed to be patentable. Since each dependent claim is also deemed to define an additional aspect of the invention, however, the individual consideration of each on its own merits is respectfully requested.

In view of the foregoing amendments and remarks, the applicants respectfully request favorable consideration and early passage to issue of the present application.

The applicants' undersigned attorney may be reached by telephone at (845) 894-3667. All correspondence should continue to be directed to the below listed address.

Respectfully submitted,



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